independent of W_S if V_B is small enough before NDR occurs. J_{tn} is more than 3 orders of magnitude larger than J_{tp} at V_B=0 V.

1. A semiconductor transistor device, comprising:

a) one or more conductive base regions connected to a first electrical terminal;

b) a first semiconductor barrier region in contact with the one or more conductive base regions, wherein a first Schottky barrier junction is formed at the interface of the first semiconductor barrier region and the one or more conductive base regions;

c) a second semiconductor barrier region in contact with the one or more conductive base regions, wherein a second Schottky barrier junction is formed at the interface of the second semiconductor barrier region and the one or more conductive base regions;

d) a conductive emitter region in contact with the first semiconductor barrier region, wherein a third Schottky barrier junction is formed at the interface of the conductive emitter region and the first semiconductor barrier region, wherein the conductive emitter region is connected to a second electrical terminal; and

e) a conductive collector region in contact with the second semiconductor barrier region, wherein a fourth Schottky barrier junction is formed at the interface of the conductive collector region and the second semiconductor barrier region, wherein the conductive collector region is connected to a third electrical terminal,

wherein at least one of the first semiconductor barrier region or the second semiconductor barrier region comprises a dimension smaller than 100 Å.

2. The semiconductor transistor device of claim **1**, wherein the first semiconductor barrier region comprises a first layer sandwiched between the one or more conductive base regions and the conductive emitter region, wherein the first layer is thinner than 100 Å.

3. The semiconductor transistor device of claim **2**, wherein the first layer comprises silicon, wherein the first layer is parallel to a (100) or (110) crystal plane.

4. The semiconductor transistor device of claim **1**, wherein the second semiconductor barrier region comprises a second layer sandwiched between the one or more conductive base regions and the conductive collector region, wherein the second layer is thinner than 100 Å.

5. The semiconductor transistor device of claim **1**, wherein the first semiconductor barrier region or the second semiconductor barrier region comprises a semiconductors material selected from the group consisting of silicon, germanium, and III-V compound semiconductors.

6. The semiconductor transistor device of claim **1**, wherein at least one of the first semiconductor barrier region or the second semiconductor barrier region has a layered structure having a thinness thinner than 50 Å.

7. The semiconductor transistor device of claim **1**, wherein a quantum well is formed in the one or more conductive base regions between barriers provided by the first semiconductor barrier region and the second semiconductor barrier region.

8. The semiconductor transistor device of claim **1**, wherein the one or more conductive base regions are configured to produce a tunneling current through the first semiconductor barrier region and the second semiconductor barrier region in response to a voltage applied to the one or more conductive base regions.

9. The semiconductor transistor device of claim **8**, wherein the work function in the one or more conductive base regions is closer to the conduction band edge than to the valence band edge in at least one of the first semiconductor barrier region or the second semiconductor barrier region, wherein the tunnel current has electrons as majority carriers.

10. The semiconductor transistor device of claim **9**, wherein the voltage applied to the is positive relative to the emitter voltage.

11. The semiconductor transistor device of claim **9**, wherein the one or more conductive base regions comprise a layer of $NiSi_2$ thinner than 20 Å.

12. The semiconductor transistor device of claim **11**, wherein the layer of $NiSi_2$ is parallel to (100) crystal plane.

13. The semiconductor transistor device of claim **8**, wherein the work function in the one or more conductive base regions is closer to the valence band edge than to the conduction band edge in at least one of the first semiconductor barrier region or the second semiconductor barrier region, wherein the tunneling current has holes as majority carriers.

14. The semiconductor transistor device of claim **13**, wherein the voltage applied to the one or more conductive base regions is negative relative to the emitter voltage.

15. The semiconductor transistor device of claim **13**, wherein the one or more conductive base regions comprise a layer of $CoSi_2$ thinner than 20 Å.

16. The semiconductor transistor device of claim **15**, wherein the layer of $CoSi_2$ is parallel to (100) crystal plane.

17. The semiconductor transistor device of claim **1**, wherein at least one of the first semiconductor barrier region or the second semiconductor barrier region is substantially undoped.

18. The semiconductor transistor device of claim **1**, wherein the conductive emitter region, the one or more conductive base regions, or the conductive collector region comprises one or more of a metal, a silicide compound, a germanide compound, or a metallic compound.

19. The semiconductor transistor device of claim **1**, wherein at least one of the first semiconductor barrier region or the second semiconductor barrier region comprises a Si/Ge heterojunction structure.

20. The semiconductor transistor device of claim **19**, wherein the Si/Ge heterojunction structure has a combined thickness smaller than 60 Å.

21. The semiconductor transistor device of claim **1**, wherein the one or more conductive base regions comprises:

a) a first conductive base region in contact with the first semiconductor barrier region;

b) a semiconductor base barrier region in contact with the first conductive base region; and

c) a second conductive base region in contact with the second semiconductor barrier region.

22. A semiconductor transistor device, comprising:

a) one or more conductive base regions;

b) a first semiconductor barrier region in contact with the one or more conductive base regions, wherein a first Schottky barrier junction is formed at the interface of the first semiconductor barrier region and the one or more conductive base regions;

c) a second semiconductor barrier region in contact with the one or more conductive base regions, wherein a second Schottky barrier junction is formed at the interface of the second semiconductor barrier region and the one or more conductive base regions;